Amendments to the Specification:

Page 5, lines 16-17: Replace the original paragraph with the following new paragraph:

FIG. 3 is a block diagram of the architecture of the packet switch with [[3]] 4 input ports, [[4]] 3 output ports, and a 10- register packet buffer according to the present invention;

Page 12, lines 2-14: Replace the original paragraph with the following new paragraph:

FIG. 3 shows the architecture of a ~~3x4~~ 4×3 packet switch with a 10-register packet buffer **106** according to the present invention. Consider the processing of, say, the third packet P(t, 3) in frame **212** of FIG. 2B. Prior to the arrival of this packet in frame **212**, it is supposed that Register 9 is available for assignment as determined by register selector **134** in frame **211**. The identity of Register 9, i.e., the numerical value "9", is conveyed to hopper **332-3** in frame **211** as being the register able to accept the third packet in the next frame **212**. Upon the arrival of new packets in frame **212**, register selector **134**, via path **142**, signals input module **112** to switch the third incoming packet to Register 9, that is, the packet arriving on lead "3" of input **302** is bit-pipelined into Register 9 using bit clock **230** during frame **212**. Moreover, the header from this third packet is conveyed to hopper **332-3** via input module **112**; an illustrative manner of accomplishing this will be discussed shortly. Incidentally, input module **112** may be, for example, a conventional 4×10 crossbar switch.